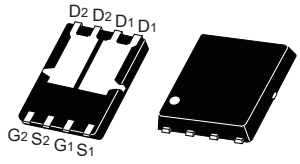
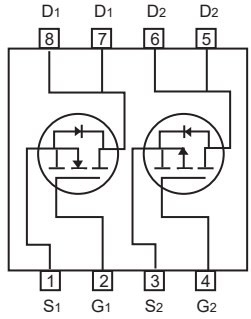
CEZ100R19

Dual Enhancement Mode Field Effect Transistor (N and P Channel)

FEATURES

- 100V, 10A, $R_{DS(ON)}$ = 100mΩ @V_{GS} = 10V.
- -100V, -6A, $R_{DS(ON)}$ = 250mΩ @V_{GS} = -10V.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handing capability.
- RoHS compliant.
- Surface mount Package.





P-PAK 5X6

ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise noted

Parameter	Symbol	N-Channel	P-Channel	Units
Drain-Source Voltage	V_{DS}	100	-100	V
Gate-Source Voltage	V_{GS}	±20	±20	V
Drain Current-Continuous	I_D @$R_{\theta JC}$	10	-6	A
	I_D @$R_{\theta JA}$	4.1	-2.6	A
Drain Current-Pulsed [a]	I_{DM} @$R_{\theta JC}$	40	-24	A
	I_{DM} @$R_{\theta JA}$	16.4	-10.4	A
Maximum Power Dissipation	P_D	17.86	17.86	W
Operating and Store Temperature Range	T_J,T_{stg}	-55 to 150		°C

Thermal Characteristics

Parameter	Symbol	Limit		Units
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	7	7	°C/W
Thermal Resistance, Junction-to-Ambient [b]	$R_{\theta JA}$	40		°C/W

N-Channel Electrical Characteristics T_A = 25°C unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250μA	100			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100V, V_{GS} = 0V			1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	V_{GS} = 20V, V_{DS} = 0V			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	V_{GS} = -20V, V_{DS} = 0V			-100	nA
On Characteristics [c]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250μA	2		4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D =3A		83	100	mΩ
Dynamic Characteristics [d]						
Input Capacitance	C_{iss}	V_{DS} = 25V, V_{GS} = 0V, f = 1.0 MHz		725		pF
Output Capacitance	C_{oss}			80		pF
Reverse Transfer Capacitance	C_{rss}			45		pF
Switching Characteristics [d]						
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 50V, I_D = 1A, V_{GS} = 10V, R_{GEN} = 6Ω		14		ns
Turn-On Rise Time	t_r			4		ns
Turn-Off Delay Time	$t_{d(off)}$			27		ns
Turn-Off Fall Time	t_f			4		ns
Total Gate Charge	Q_g	V_{DS} = 80V, I_D = 2.1A, V_{GS} = 10V		15		nC
Gate-Source Charge	Q_{gs}			2.4		nC
Gate-Drain Charge	Q_{gd}			5.1		nC
Drain-Source Diode Characteristics and Maximun Ratings						
Drain-Source Diode Forward Current [b]	I_S				10	A
Drain-Source Diode Forward Voltage [c]	V_{SD}	V_{GS} = 0V, I_S = 1.5A			1.3	V

Notes :
a.Repetitive Rating : Pulse width limited by maximum junction temperature.
b.Surface Mounted on FR4 Board, t ≤ 10 sec.
c.Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
d.Guaranteed by design, not subject to production testing.

P-Channel Electrical Characteristics $T_A = 25^{\circ}C$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-100			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -100V, V_{GS} = 0V			-1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	V_{GS} = 20V, V_{DS} = 0V			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	V_{GS} = -20V, V_{DS} = 0V			-100	nA
On Characteristics [c]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = -250μA	-2		-4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = -10V, I_D =-4A		207	250	mΩ
Dynamic Characteristics [d]						
Input Capacitance	C_{iss}	V_{DS} = -15V, V_{GS} = 0V, f = 1.0 MHz		680		pF
Output Capacitance	C_{oss}			100		pF
Reverse Transfer Capacitance	C_{rss}			60		pF
Switching Characteristics [d]						
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = -80V, I_D = -7A, V_{GS} = -10V, R_{GEN} = 6Ω		13		ns
Turn-On Rise Time	t_r			7		ns
Turn-Off Delay Time	$t_{d(off)}$			29		ns
Turn-Off Fall Time	t_f			5		ns
Total Gate Charge	Q_g	V_{DS} = -80V, I_D = -7A, V_{GS} = -10V		16		nC
Gate-Source Charge	Q_{gs}			2		nC
Gate-Drain Charge	Q_{gd}			6		nC
Drain-Source Diode Characteristics and Maximun Ratings						
Drain-Source Diode Forward Current [b]	I_S				-6	A
Drain-Source Diode Forward Voltage [c]	V_{SD}	V_{GS} = 0V, I_S = -1A			-1.2	V

Notes :
a.Repetitive Rating : Pulse width limited by maximum junction temperature.
b.Surface Mounted on FR4 Board, t ≤ 10 sec.
c.Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
d.Guaranteed by design, not subject to production testing.

N-CHANNEL

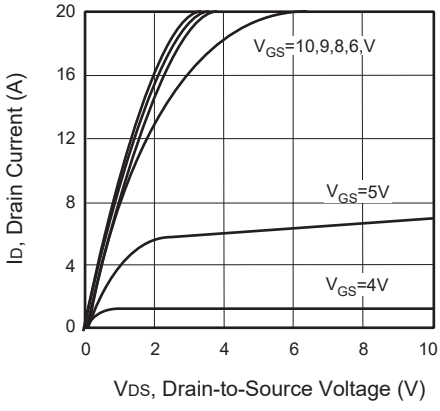


Figure 1. Output Characteristics

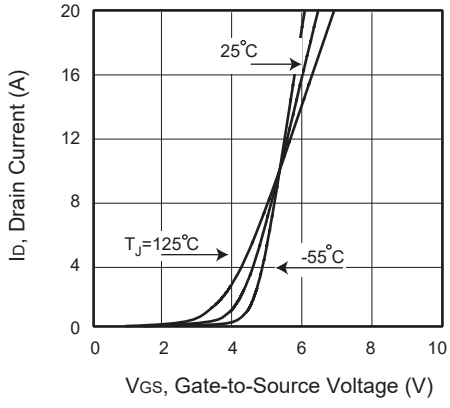


Figure 2. Transfer Characteristics

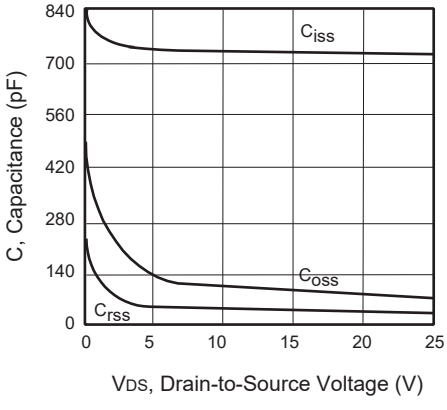


Figure 3. Capacitance

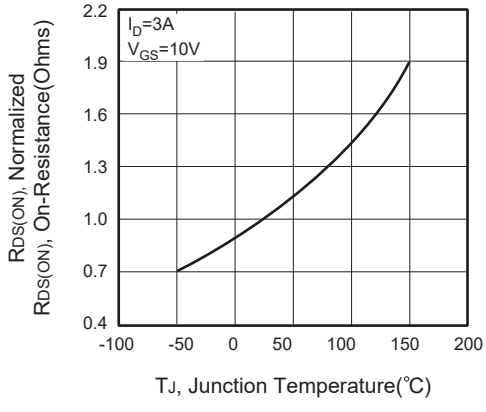


Figure 4. On-Resistance Variation with Temperature

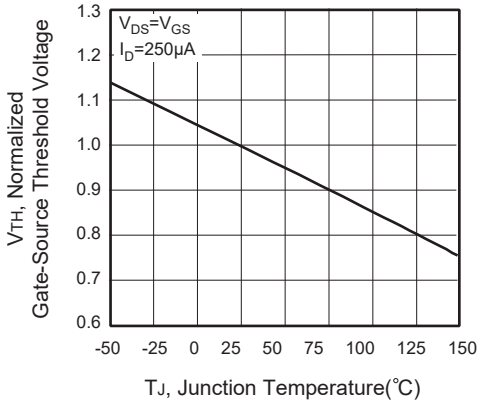


Figure 5. Gate Threshold Variation with Temperature

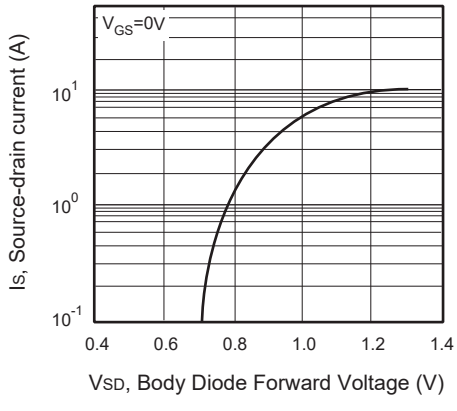


Figure 6. Body Diode Forward Voltage Variation with Source Current

P-CHANNEL

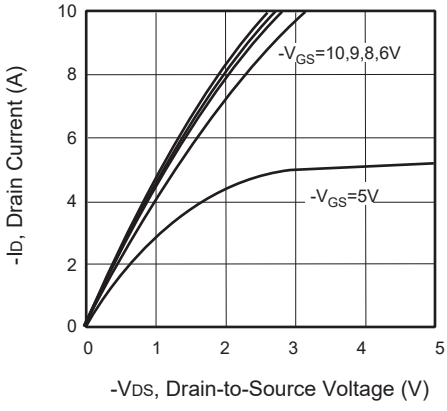


Figure 7. Output Characteristics

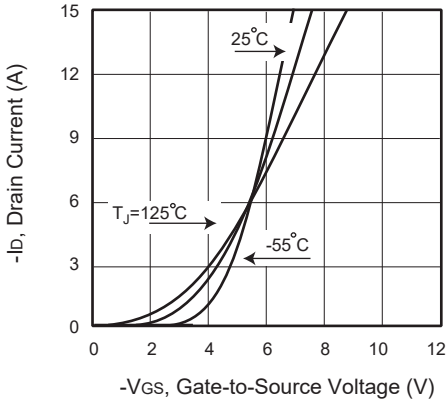


Figure 8. Transfer Characteristics

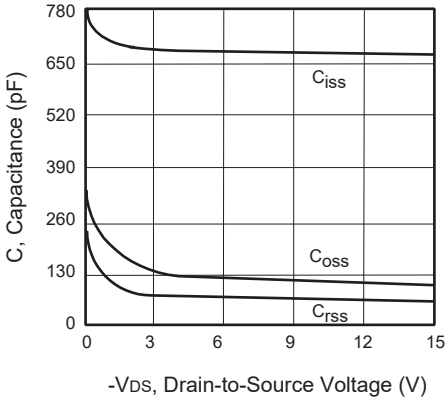


Figure 9. Capacitance

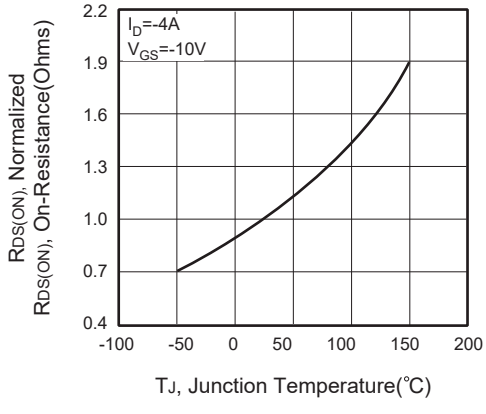


Figure 10. On-Resistance Variation with Temperature

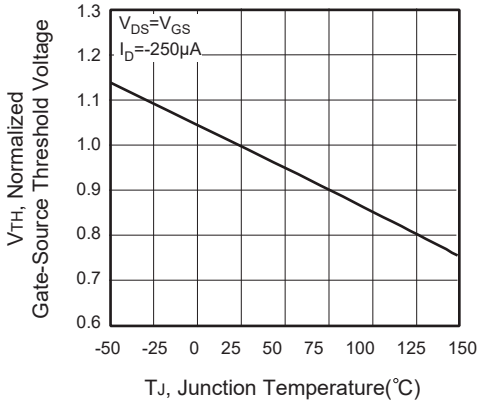


Figure 11. Gate Threshold Variation with Temperature

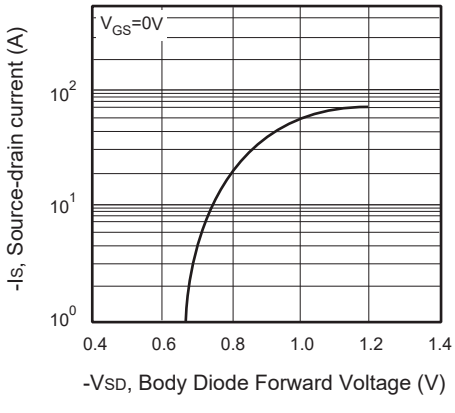


Figure 12. Body Diode Forward Voltage Variation with Source Current

N-CHANNEL

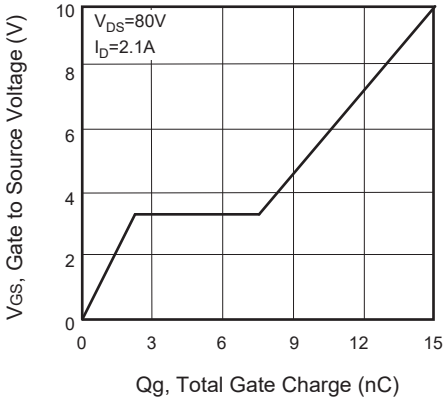


Figure 13. Gate Charge

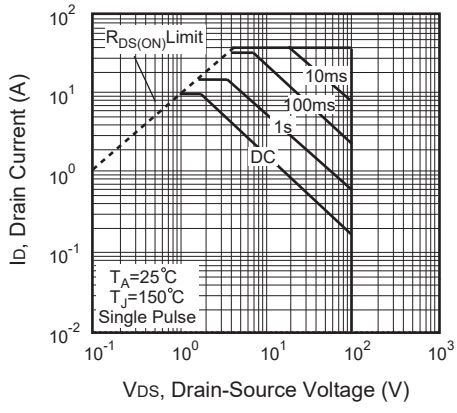


Figure 14. Maximum Safe Operating Area

P-CHANNEL

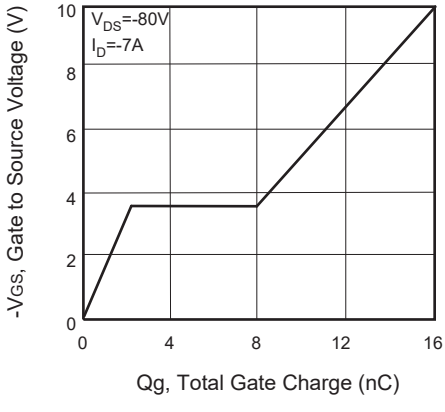


Figure 15. Gate Charge

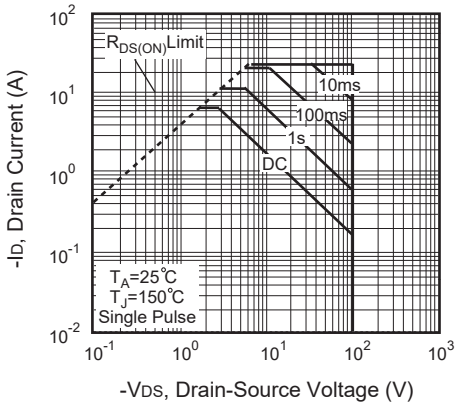


Figure 16. Maximum Safe Operating Area

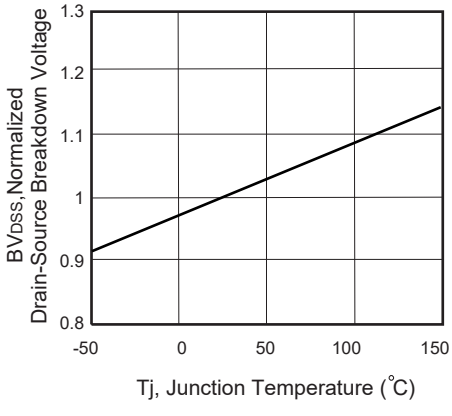


Figure 17. Breakdown Voltage Variation VS Temperature

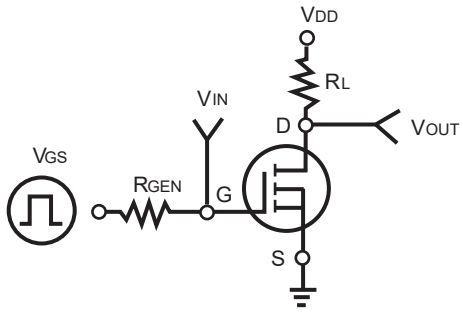


Figure 18. Switching Test Circuit

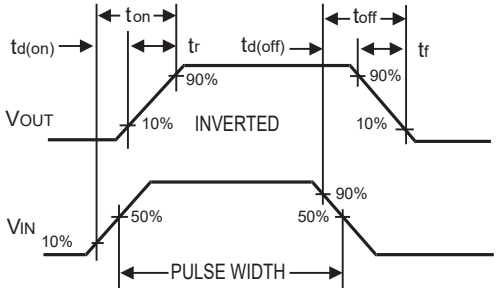


Figure 19. Switching Waveforms

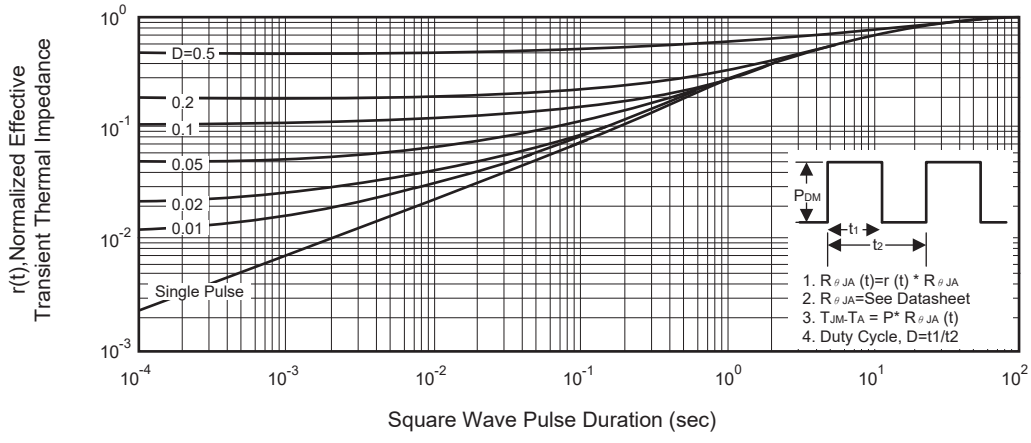


Figure 20. Normalized Thermal Transient Impedance Curve